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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
THAI, TUAN V	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 06/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/038,941	MASTRONARDE ET AL.	
	Examiner	Art Unit	
	Tuan V. Thai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-6,9-11,13-15 and 18-36* is/are pending in the application.

4a) Of the above claim(s) *3,7,8,12,16 and 17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-6,9-11,13-15 and 18-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Specification

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 28, 2004 has been entered.

2. Claims 1-2, 4-6, 9-11, 13-15 and 18-36 are presented for examination. Claims 3, 7-8, 12, 16 and 17 have been cancelled.

3. Applicant is reminded of the duty to fully disclose information under 37 CFR 1.56.

4. The non-statutory double patenting rejection is hereby maintained since claims 1-16 of patent application 10/033,440 (now patent 6,792,516) contains every element of claims 1-2, 4-6, 9-11, 13-15 and 18-36 of the instant application and as such anticipates claims 1-2, 4-6, 9-11, 13-15 and 18-36 of the instant application. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claims in the current application are slightly broader in their

new form as being compared to the limitations of the original claims. Examples are: Claims 1, 6, 10, 15, 19, 24, 28 and 33 of the current application are still obvious slight variation of claims 1, 5, 9 and 13 of patent 6,792,516. The claims are not patentably distinct from each other because the claims are directed to the same method and system (memory arbiter) with a memory device and controller *configured to service the lower priority requests for a predetermined period if incoming higher priority request is directed to the same page of memory as the current lower priority requests.*

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-2, 4-6, 9-11, 13-14 are rejected under 35 U.S.C. § 102(b) as being anticipated by Lewchuk et al. (USPN: 6,058,461); hereinafter Lewchuk.

As per claims 1 and 6; Lewchuk teaches the invention as claimed including a method and a memory arbiter for servicing data in a computer system comprising a memory area is taught as

open page/priority storage 48 (e.g. see figure 2; column 8, lines 19-20); a memory controller coupled to the memory area is taught as memory controller 42 having a control unit 46 for receiving memory requests and corresponding priorities from a microprocessor (e.g. see figure 2; column 5, line 61 bridging column 6, line 22; also column 8, lines 54 et seq.); Lewchuk further discloses the lower priority request is interrupted to serve higher priority request (e.g. see column 6, lines 11 et seq.; column 9, lines 45 et seq.) and wherein the memory controller is configured to continue to service current lower priority requests for ***a first predefined period*** if an incoming higher priority request is directed to a same page of memory as the current lower priority requests is taught by Lewchuk; for example, starting at column 6, lines 63 et seq.; Lewchuk discloses to interrupt a memory operation to perform a higher priority memory operation comprises inserting the beats for the higher priority memory operation between ***two of the beats/cycles out of the four cycles*** (first predetermined period) for the lower priority memory operation; therefore the lower priority is still allowed to perform at least for a predefined period of at least two cycles before service the higher priority requests; and to subsequently service the higher priority for a predetermined second period (e.g. the remaining two cycles of the four clock cycles); by these rationales, claims 1 and 6 are rejected.

As per claim 2, it's inherent that any requests from the

same agent (either microprocessor A or microprocessor B) which generates the lower priority request are served during the first period (the first two cycles of the four clock cycles as detailed above in claim 1) in the system of Lewchuck (e.g. column 6, line 47 et seq. bridging column 7, line 11);

As per claims 4 and 9, Lewchuk discloses the memory controller unit 46 is configured to eventually resume servicing any lower priority requests (in-progress memory operation) after the high priority request is processed (e.g. see column 8, lines 65-68);

As per claim 5, the further limitation of first and second counters being used to monitor the predefined period is embedded in the system of Lewchuk since to determine the number of beats/cycles (being disclosed as two (2) cycles in Lewchuk's invention, e.g. see column 6, lines 64 bridging column 7, line 1) for interrupting a memory operation to perform a higher memory operation, counter(s) must be utilized to carry-out such operation; by this rationale, claim 5 is rejected.

As per claims 10-11 and 14, they encompass the same scope of invention as to that of claims 1-2 and 4, the claims are therefore rejected for the same reason as being set forth above. In addition, the processor for initiating a higher and lower priority memory requests is taught as processors 10 A,B (e.g. see figure 2, column 8, lines 11 and 38 et seq.).

Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 15 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lewchuck (USPN: 6,058,461).

As per claims 15 and 18; Lewchuck discloses the invention as claimed, detailed above with respect to claims 1-2 and 4; Lewchuck however does not particularly disclose a computer-readable medium of instructions to be implemented on a computer as being claimed in claims 15 and 18. However, one of ordinary skill in the art would have recognized that computer readable medium (i.e., floppy, cd-rom, etc.) carrying computer-executable instructions for implementing a method, because it would facilitate the transporting and installing of the method on other systems, is generally well-known in the art. For example, a copy of the Microsoft Windows operating system can be found on a cd-rom from which Windows can be installed onto other systems, which is a lot easier that running a long cable or hand typing the

software onto another system. The examiner takes Official Notice of this teaching. Therefore, it would have been obvious to put Mattson's program on a computer readable medium, because it would facilitate the transporting, installing and implementing of Lewchuck's program on other systems.

9. Claims 19-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lewchuck (USPN: 6,058,461) in view of Iizuka et al. (USPN:5,699,521), hereinafter Iizuka.

As per claims 19 and 24, Lewchuk teaches the invention as claimed including a method and a memory arbiter for servicing data in a computer system comprising a memory area is taught as open page/priority storage 48 (e.g. see figure 2; column 8, lines 19-20); a memory controller coupled to the memory area is taught as memory controller 42 having a control unit 46 for receiving memory requests and corresponding priorities from a microprocessor (e.g. see figure 2; column 5, line 61 bridging column 6, line 22; also column 8, lines 54 et seq.); Lewchuk; however does not particularly disclose the memory controller is configured to interrupt servicing of higher priority requests after a predefined number are processed to process lower priority requests for a predefined period of time. Iizuka, in his teaching of communication system and method, clearly discloses the missing elements that is known to be required in Lewchuk in order to arrive at Applicant's current invention wherein Iizuka

discloses interrupting high priority servicing-data-request to allowing passing/servicing of nonpriority or low priority data request in order to prevent or keep the nonpriority or low priority data request from starvation (e.g. see column 11, lines 12-53). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to look into the invention of Iizuka in order to utilize the teaching of "interrupting the higher priority service to allow for servicing of the lower priority requests" for that of Lewchuk invention. In doing so, it would enhance system reliability, and allow for continuously/uninterrupted servicing of system requests; since Iizuka clearly teaches that it would prevent or keep the nonpriority/low priority data requests from starvation; therefore being advantageous.

As per claims 20 and 25, Lewchuk discloses wherein the memory controller is configured to redefine the status of the higher priority requests to a lower priority status after a predefined number are processed (e.g. see column 8, lines 61 et seq.);

As per claims 21-22 and 26-27, the reinstatement of the higher priority requests to its initial priority status after the lower priority request is processed, and resuming the service of higher priority requests after the predefined period expires is taught by the Lewchuk as being equivalent to the control unit 46 resume the in-progress memory operation after completing the

memory operation (e.g. column 8, lines 65-68);

As per claim 23, see arguments with respect to claim 5, in addition, it should be noted that Iizuka also discloses a counter for monitoring the number of high priority requests as being equivalent to the upper limit numbers of continuous fetch times of the queues and the current number of continuous fetch times of the queues ***are used to count the number of continuous fetch times of the priority data with the current number of continuous fetch times*** (e.g. see column 11, lines 14 et seq.);

As per claims 28-32, they encompass the same scope of invention as to that of claims 19-23, the claims are therefore rejected for the same reason as being set forth above. In addition, the processor for initiating a higher and lower priority memory requests is taught as processors 10A,B (e.g. see figure 2, column 8, lines 11 and 38 et seq.).

As per claims 33-36; the combination of Lewchuck and Iizuka disclose the invention as claimed, detailed above with respect to claims 19-32; Lewchuck and Iizuka however do not particularly disclose a computer-readable medium of instructions to be implemented on a computer as being claimed in claims 19-32. However, one of ordinary skill in the art would have recognized that computer readable medium (i.e., floppy, cd-rom, etc.) carrying computer-executable instructions for implementing a method, because it would facilitate the transporting and installing of the method on other systems, is generally well-

known in the art. For example, a copy of the Microsoft Windows operating system can be found on a cd-rom from which Windows can be installed onto other systems, which is a lot easier that running a long cable or hand typing the software onto another system. The examiner takes Official Notice of this teaching. Therefore, it would have been obvious to put Mattson's program on a computer readable medium, because it would facilitate the transporting, installing and implementing of Lewchuck and Iizuka's program on other systems.

10. As to the remark; Applicant's counsel argued that (a) the pending claims of the present application are patently distinct from and are not obvious slight variations of claims 1-16 of Mastronarde (6,792,516) (remark, pages 8-10) (b) Lewchuck fails to disclose first and second predetermined periods (remark, page 10); (c) The combination of Lewchuck and Iizuka do not disclose interrupting servicing of high priority requests after predefined number are processed to process lower priority requests for a predetermined period of time, Iizuka only discloses interrupting fetches of priority data with the fetching of nonpriority data (amendment's page 12).

With respect to (a); as previously indicated, although the conflicting claims are not identical, they are not patentably distinct from each other because the claims of patent 6,792,516 and current application are directed to the same invention of

managing/arbitrating memory requests by *configuring the memory controller to service the lower priority requests for a predetermined period if incoming higher priority request is directed to the same page of memory as the current lower priority requests*. With respect to (b), the first and second periods which allocated for the lower and higher priority request are equivalent taught by Lewchuk as the first two cycles and the remaining two cycles of the four clock cycles that being allocating for servicing the lower and higher priority requests wherein ***the lower priority is still allowed to perform at least for a predefined period of at least two cycles*** before service the higher priority as being contended by Applicant's counsel (e.g. see Lewchuk's column 6, lines 63 et seq.). With respect to (c), it should be noted that, the Iizuka reference ('521) cited by Examiner for teaching the missing element of the memory controller is configured ***to interrupt servicing of higher priority requests*** after a predetermined number are processed to process lower priority requests, and in considering a 35 USC 103 rejection, it is not strictly necessary that a reference or references explicitly suggest the claimed invention (this is tantamount to a 35 USC 102 reference if the modifications would have been obvious to those of ordinary skill in the art. It has been held that the test of obviousness is not whether the features of a secondary reference may be bodily incorporated into the primary references' structure, nor whether the claimed

invention is expressly suggested in any one or all of the references; rather, the test is what the combined teachings of the reference would have suggested to those of ordinary skill in the art. See In re Keller et al., 208 U.S.P.Q 871. In addition, Examiner further recognizes that references cannot be arbitrarily combined and that there must be some reason why one skilled in the art would be motivated to make the proposed combination of primary and secondary references. In re Nomiya, 184 USPQ 607 (CCPA 1975). However, there is no requirement that a motivation to make the modification be expressly articulated. The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re McLaughlin, 170 USPQ 209 (CCPA 1971). Lewchuck and Iizuka references are evaluated by what they suggest to one versed in the art, rather than by their specific disclosures. In re Bozek, 163 USPQ 545 (CCPA) 1969. In this case, the Iizuka reference was used to provide evidence of ***interrupting high priority servicing-data-request to allowing passing/servicing of nonpriority or low priority data request in order to prevent or keep the nonpriority or low priority data request from starvation*** (e.g. see column 11, lines 12-53). The combination would enhance system reliability by allow for continuously/uninterrupted servicing of system requests since Iizuka clearly teaches that it would prevent or keep the nonpriority/low priority data requests from starvation. The 35 USC § 103 rejection based on said combination of Lewchuck

and Iizuka is therefore deemed to be proper.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V. Thai whose telephone number is (571)-272-4187. The examiner can normally be reached on from 6:30 A.M. to 4:00 P.M. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew M. Kim can be reached on (571)-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see ***http://pair-direct.uspto.gov***. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVT/June 07, 2005

Tuan V. Thai
PRIMARY EXAMINER
Group 2100